Data Sheet

2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

Features

- Serial Data Rate up to 2.5 Gb/s
- 16-bit Wide ECL 100K Compatible Parallel Data Interface
- Differential High Speed Data Outputs
- Differential or Single-ended High Speed Data and Clock Inputs
- On-chip Phase Detector (VS8061 Multiplexer)
- Power Dissipation: VS8061: 2.0W(max), VS8062: 1.7W(max)
- Standard ECL Power Supplies: V_{EE} = -5.2 volts, V_{TT} = -2.0 volts
- Commercial (0° to 70° C) or Industrial (-40° C to 85° C) Temperature Range
- Available in 52-pin Ceramic Leaded Chip Carrier Package or 52-pin Plastic Quad Flat Pack

Functional Description

The VS8061 and VS8062 are high speed interface devices capable of data rates up to 2.5 Gb/s. These devices are fabricated in gallium arsenide using the Vitesse H-GaAs E/D MESFET process to achieve high speed and low power dissipation. For ease of system design using these products, both devices use industry standard, -5.2V and -2V, power supplies, and have ECL compatible I/O for parallel data interfaces. Typical applications include telecommunication transmission and instrumentation.

VS8061 Multiplexer

The VS8061 consists of a 16:1 multiplexer circuit, a phase detector, and a timing circuit which generates a divide-by-16 clock from the high speed clock input. The 16:1 multiplexer accepts 16 parallel single-ended ECL compatible inputs (D0..D15) at data rates up to 156Mb/s and bitwise serializes them into a 2.5Gb/s serial output (DO/DON). The internal timing of the VS8061 is referenced to the negative going edge of the high speed clock true input (CLK). This clock is divided by 16 and is provided as an output (CLK16/CLK16N). The setup and hold time of the parallel inputs (D0..D15) are specified with respect to the falling edge of CLK16, so that CLK16/CLK16N can be used to clock the data source of D0..D15. The on-chip phase detector monitors the phase relationship between the internally generated divide by 16 clock and an externally supplied low speed reference clock input (DCLK/DCLKN). Phase difference between these two clock signals generates an up or down output (U, D) for phase lock applications. The phase detector can be used as part of an external Phase Locked Loop (PLL) to implement a clock multiplication function.

In applications where a 2.5 GHz system clock is provided, and the phase detector function is not required, it is recommended to connect one side of the DCLK/DCLKN input to V_{TT} through a 50 ohm resistor. The U and D output can be left open and unused.

VS8062 Demultiplexer

The VS8062 consists of a 1:16 demultiplexer and timing circuitry which generates a divide-by-16 clock from the high speed clock input. The demultiplexer accepts a serial data stream input (DI/DIN) at up to 2.5Gb/s and deserializes it into 16 parallel single-ended ECL compatible outputs (D0..D15) at data rates up to 156 Mb/s. The internal timing of the VS8062 is referenced to the negative going edge of the high speed clock true input (CLK). This clock is divided by 16 and provided as an output (CLK16/ CLK16N). The timing parameters of the parallel data outputs (D0..D15) are specified with respect to the falling edge of CLK16, so that CLK16/ CLK16N can be used to clock the destination of D0..D15.

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Figure 1: VS8061 Block Diagram

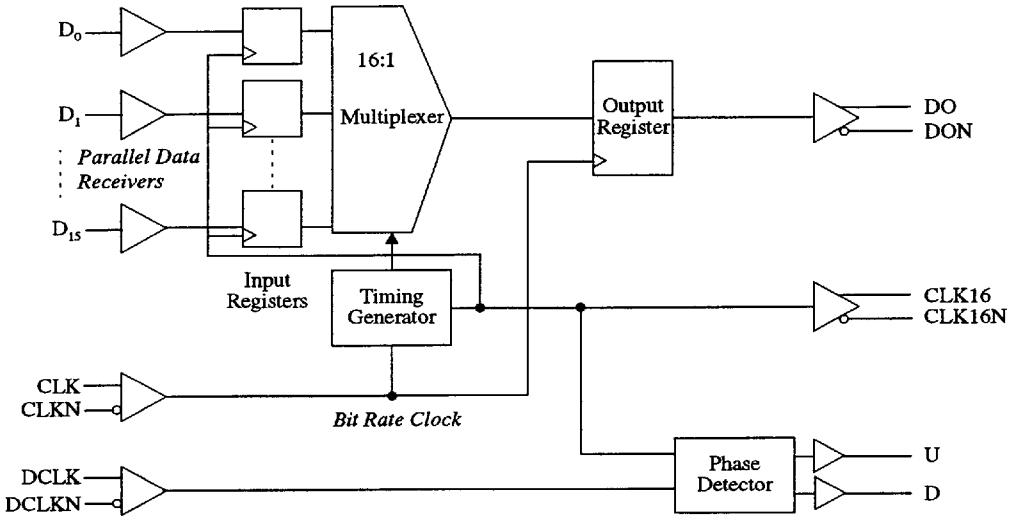
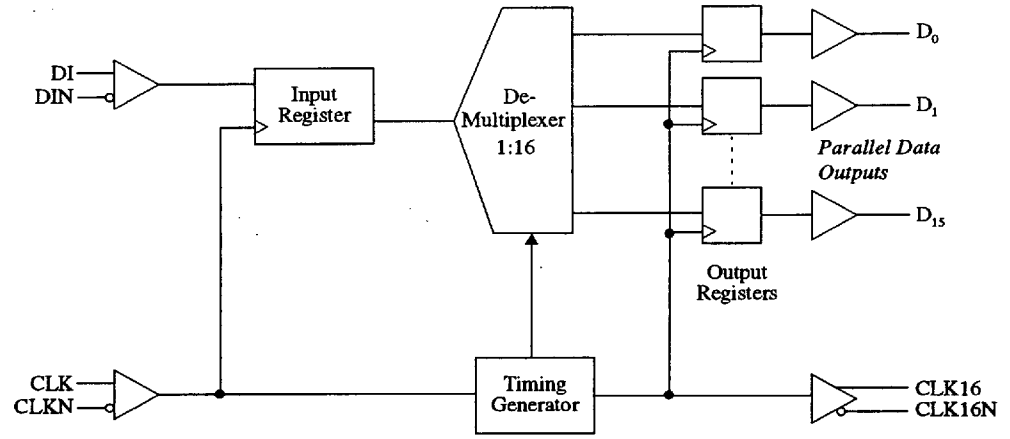


Figure 2: VS8062 Block Diagram



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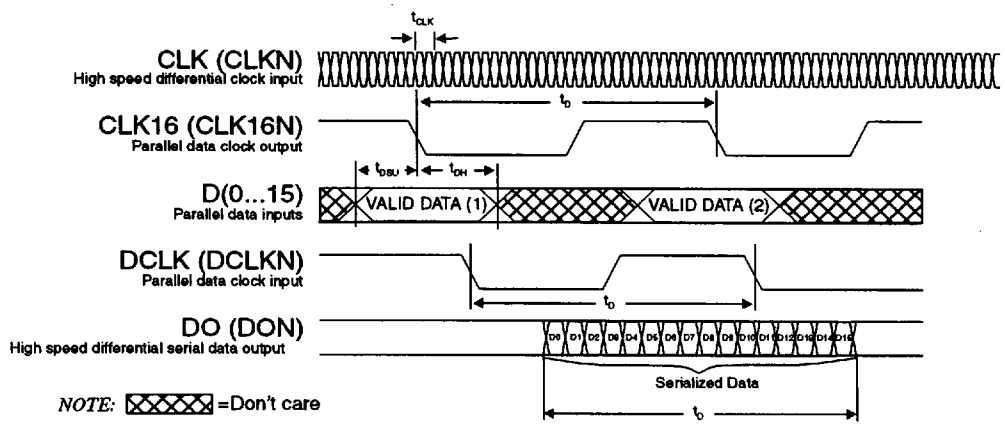
VS8061 Multiplexer AC Characteristics *(Over recommended operating range)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	Clock period*	400	-	-	ps
t_D	CLK16, DCLK period (t_{CLK} x 16)	6.4	-	15.6	ns
t_{DSU}	Parallel data set-up time (wrt CLK16 falling edge)	2.0	-	-	ns
t_{DH}	Data hold time (wrt CLK16 falling edge)	0.5	-	-	ns
t_{DC}	CLK16 duty cycle	40	-	60	%
t_r, t_f	DCLK (DCLKN) rise and fall times (10%-90%)	-	-	1.5	ns
t_r, t_f	D(0..15) rise and fall times (10%-90%)	-	-	2.0	ns
t_r, t_f	CLK16 (CLK16N) rise and fall times (10%-90%)	-	0.5	1	ns
t_r, t_f	DO (DON) rise and fall times (20%-80%)	-	150	165	ps

**The parts are guaranteed to operate to a maximum frequency of 2.5GHz.*

Figure 3: VS8061 Multiplexer Waveforms



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VS8061 Phase Detector Logic Diagram

The phase detector inside the VS8061 compares the phase difference between the internally generated divide-by-16 clock and the DCLK input. If both inputs (CLK16 and DCLK) to the phase detector are in phase, the U and D outputs will both be low. If the rising edge of CLK16 precedes DCLK, a series of pulses with pulse widths proportional to the phase difference will be present at the U output. Conversely, if DCLK precedes CLK16, then a series of pulses with widths proportional to the phase difference will be present at the D output. The other output will remain low. The Phase Detector ignores phase differences for falling edges. This circuitry is useful for implementing a Clock Multiplier Unit (CMU) function with the VS8061. For example, the DLCK can be the system reference clock at the parallel data rate. An external Voltage Controlled Oscillator (VCO) at 16X the frequency of the reference clock can be used as the CLK input for the VS8061. The phase detector outputs (U and D) can then be used by an external integrator to generate an output that controls the VCO. The generated 16X clock from the VCO will be phase-locked to the reference clock.

Figure 4: VS8061 Phase Detector Logic Diagram

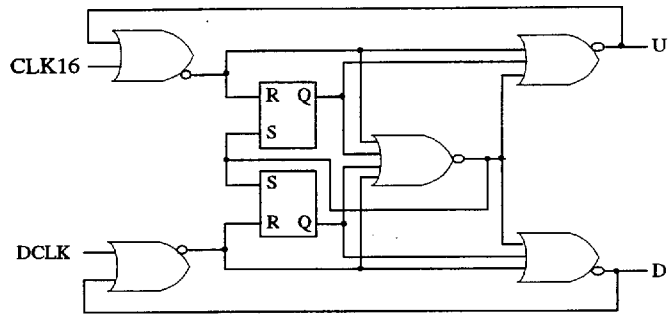
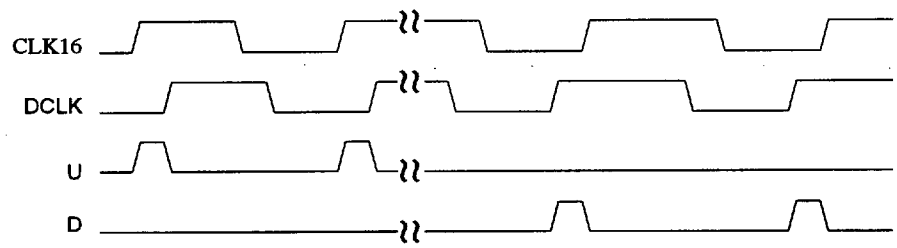


Figure 5: Phase Detector Input and Output Waveforms



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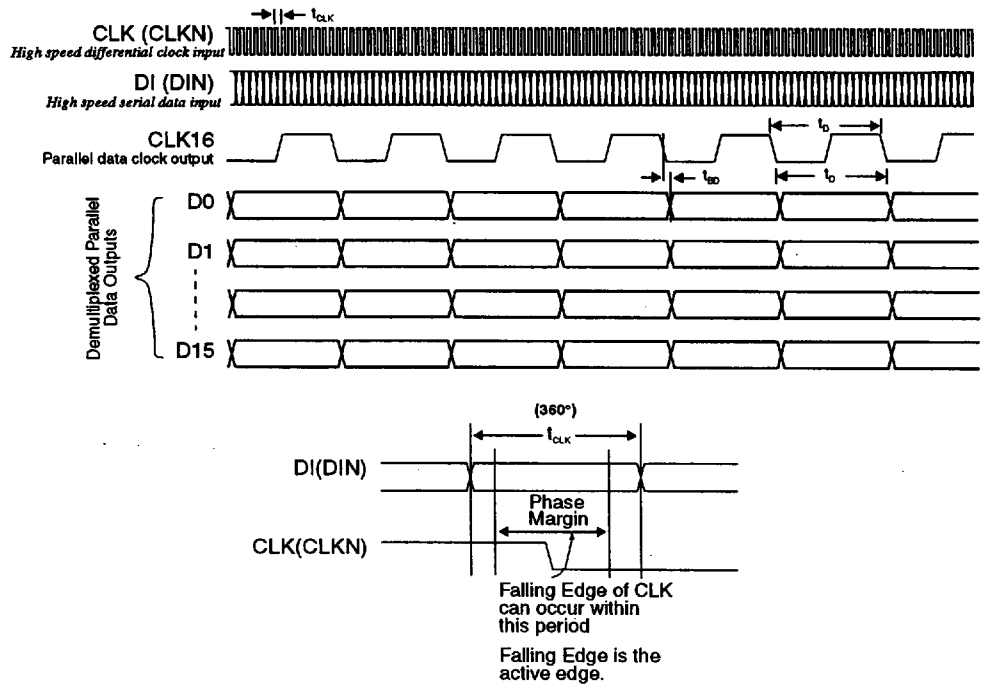
VS8062 Demultiplexer AC Characteristics *(Over recommended operating range)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	Clock period[1]	400	-	-	ps
t_D	BYTE CLK16 period (t_{CLK} x 16)	6.4	-	-	ns
t_{BD}	CLK16 falling edge output to valid data	1.0	-	3.0	ns
phase margin	Serial data phase timing margin with respect to high speed clock: Phase Margin[3] = $\left(1-\frac{t_{SU}+t_H}{t_{CLK}}\right)\times 360°$	180[2]	-	-	degrees

(1) If t_{CLK} changes, all the remaining parameters change as indicated by the equations.
(2) At t_{CLK} = 400ps.
(3) t_{SU} and t_H are setup and hold times of the serial data input register.

Figure 6: VS8062 Timing Diagram



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Absolute Maximum Ratings[1]

Power Supply Voltage (V_{TT}) ..... -3.0V to 0.5V
Power Supply Voltage (V_{EE}) ..... VTT + 0.7V to -7.0V
Input Voltage Applied [2] (V_{ECLIN}) ..... -2.5V to 0.5V
High Speed Input Voltage Applied [2] (V_{HSIN}) ..... VEE-0.7V to VCC+0.7V
Output Current, I_{OUT} (DC, output HI) ..... -50 mA
Case Temperature Under Bias (T_C) ..... -55° to 125°C
Storage Temperature (T_{STG}) ..... -65° to 150°C

Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) V_{TT} must be applied before the magnitude of any input signal voltage ($|V_{IN}|$, $|V_{HSIN}|$) can be greater than $|V_{TT}$ - 0.5V|

Recommended Operating Conditions

Power Supply Voltage (V_{TT}) ..... -2.0V±5 %
Power Supply Voltage (V_{EE}) ..... -5.2V±5 %
Operating Temperature Range* (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to 85°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

For performance considerations, minimum ESD protection is provided for the high speed input pins. Therefore, proper procedures should be used when handling these products. The VS8061/8062 are rated to the following ESD voltages based on the human body model:

1. All high speed input pins are rated at or above 500V.
2. All other pins are rated at or above 2000V.

The above ratings apply to both "F" and "QH" packages.

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DC Characteristics

Table 1: ECL Inputs and Outputs

(Over recommended operating conditions with internal V_{REF}, V_{CC} = GND, Output load = 50 ohms to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1100	-	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	-	-1750	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1040	-	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	-	-1600	mV	Guaranteed LOW signal for all inputs
$\Delta VECL_{OUT}$	Output voltage swing	0.850	-	-	V	Output load 50 ohm to V_{TT}
$\Delta VECL_{IN}$	Input voltage swing	0.600	0.800	1.2	V	AC coupled

Note: Differential ECL output pins must be terminated identically.

Table 2: Power Dissipation

(Over recommended operating conditions, V_{CC}= GND, outputs open circuit)

Parameter	Description	VS8061 (Max)	VS8062 (Max)	Units
I_{EE}	Power supply current from V_{EE}	260	220	mA
I_{TT}	Power supply current from V_{TT}	260	230	mA
P_D	Power dissipation	2.0	1.7	W

Table 3: High Speed Input and Output Specifications

(Over recommended operating conditions, V_{CC} = GND, Output load = 50 ohm to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{HSOUT}	Output voltage swing	0.7	0.9	-	V	Output load, 50 Ohm to -2.0V
ΔV_{HSIN}	Input voltage swing	0.6	0.7	1.2	V	AC coupled
T_r, T_f	Input voltage rise and fall time (high speed)	-	0.2	1.5	ns	same for all data rates; no worse than sine wave at max speed

Notes: 1) Built-in references generator, the high speed inputs are designed for AC coupling

2) If a high speed input is driven single-ended, a capacitor should be connected between the unused high speed or complement input and V_{TT} (see figures 7 and 8).

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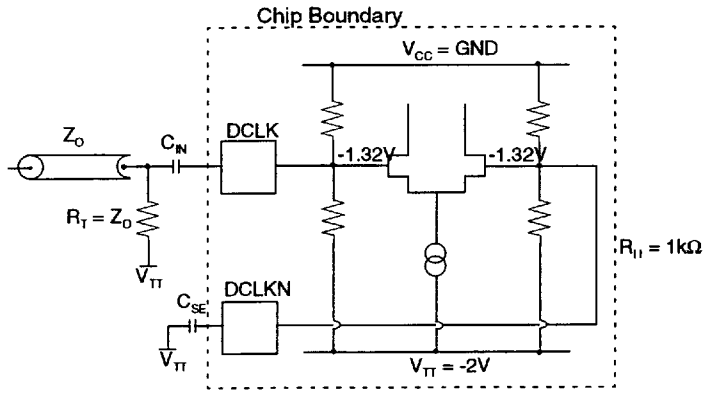
Coupling for Inputs

Figure 7: AC-Coupling for DCLK, DCLKN Inputs



C_{IN} TYP = 0.1µF

C_{SE} TYP = 0.1µF for single ended applications. (Capacitor values are selected for DCLK = 155 Mb/s.)

DCLK, DCLKN Inputs

Internal biasing will position the reference voltage of approximately -1.32V on both the true and complement inputs. This input can either be DC-coupled or AC-coupled; it can also be driven single-ended or differentially. Figure 7 shows the configuration for a single-ended, AC-coupling operation. In the case of direct coupling and single-ended input, it is recommended that a stable V_{REF} for ECL levels be used for the complementary input.

High Speed Clock and Serial Data Inputs

It is recommended that all high speed clock and serial data inputs (i.e. CLK/CLKN for the VS8061; DI/DIN and CLK/CLKN for the VS8062) be AC-coupled. Figure 8 shows the configuration for a single-ended AC-coupling operation.

In most situations these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. The following is to assist in this application.

All serial data and clock inputs have the same circuit topology, as shown in figure 8. The reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude. For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip

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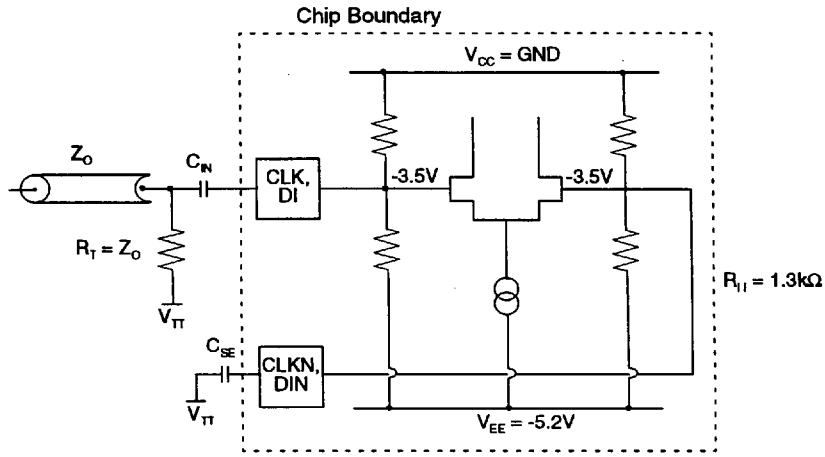
resistor divider. The external reference should have a nominal value as indicated in the table and can be connected to either side of the differential gate.

Table 4: High Speed Clock and Serial Data Inputs

Product	*Input*	*Reference*	*Min (p-p)*	*Max (p-p)*
VS8061	DCLK, DCLKN	-1.32V	600mV	1.2V
VS8061, VS8062	CLK, CLKN	-3.5V	600mV	1.2V
VS8062	DI, DIN	-3.5V	600mV	1.2V

Figure 8: High Speed Clock and Serial Data Inputs



C_{IN} TYP = 100 pF

C_{SE} TYP = 100 pF for single ended applications. (Capacitor values are selected for DI = 2.5Gb/s.)

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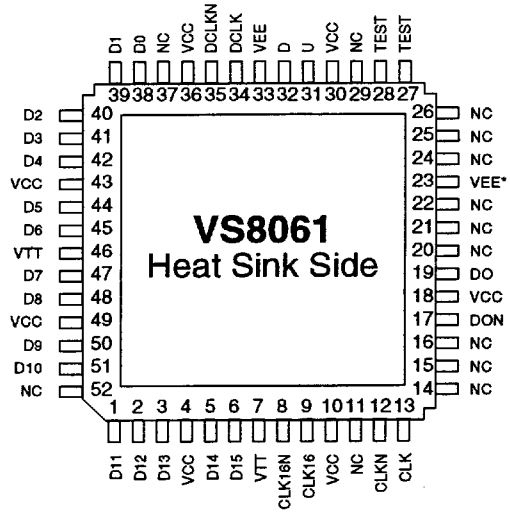
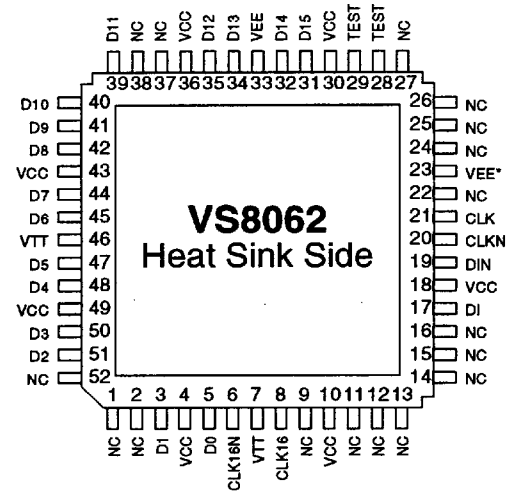
Figure 9: VS8061/8062 F (52-Pin LDCC) Pin Diagrams





Heat Sink Up
Top View

*Heat sink is electrically connected to pin 23 and should be biased to V_{EE}.

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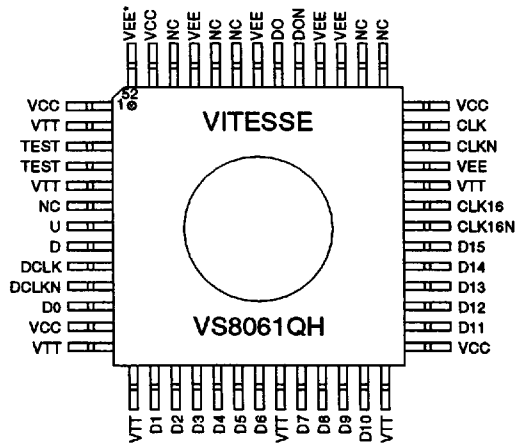
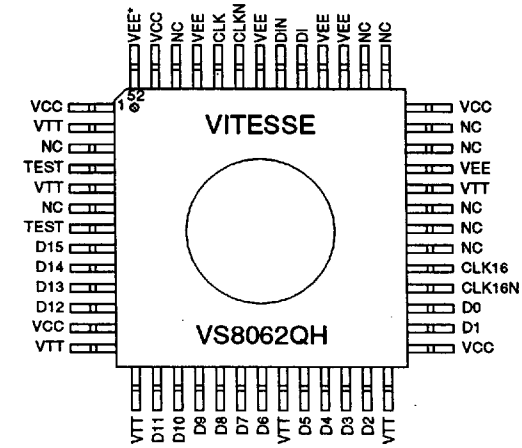
Figure 10: VS8061/8062 QH (52-Pin PQFP) Pin Diagrams





Heat Spreader Up
Top View

*Heat spreader is electrically connected to pin 52 and should be biased to V_{EE}.

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Table 5: VS8061 Pin Description

Pin # For QH	*Pin # For F*	*Name*	*I/O*	*Level*	*Description*
38	13	CLK	I	HS	High speed clock true[1]
37	12	CLKN	I	HS	High speed clock complement [1]
9	34	DCLK	I	ECL	Data clock true[1]
10	35	DCLKN	I	ECL	Data Clock complement[1]
34	9	CLK16	O	ECL	Clock divide-by-16 true
33	8	CLK16N	O	ECL	Clock divide-by-16 complement
11, 15-20, 22-25, 28-32	1-3,5,6,38-42,44,45,47, 48,50,51	D[0:15]	I	ECL	Parallel data inputs
45	19	DO	O	HS	Serial data output true
44	17	DON	O	HS	Serial data output complement
7	31	U	O	ECL	Phase detector output - up frequency
8	32	D	O	ECL	Phase detector output - down frequency
1,12,27, 39,51	4,10,18,30, 36,43,49	V_{CC}	-	-	Most positive supply
2,5,13,14,21, 26,35	7,46	V_{TT}	-	-	DCFL negative supply
36,42,43, 46, 49	33	V_{EE}	-	-	SCFL negative supply
6,40,41,47,48, 50	11,14-16,20-22,24-26,29,37,52	NC	-	-	Do not connect, leave open
3,4	27,28	Test	-	-	Test inputs. Used in factory for testing, connect to VTT through a resistor
52	23	V_{EE*}	-	-	Heat sink bias, connect to V_{EE}

[1] *Can be used single-ended.*

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Table 6: VS8062 Pin Description

Pin # For QH	*Pin # For F*	*Name*	*I/O*	*Level*	*Description*
48	21	CLK	I	HS	High speed clock true [1]
47	20	CLKN	I	HS	High speed clock complement [1]
44	17	DI	I	HS	Serial data true [1]
45	19	DIN	I	HS	Serial data complement [1]
31	8	CLK16	O	ECL	Parallel data clock (high speed clock divide-by-16) true
30	6	CLK16N	O	ECL	Parallel data clock (high speed clock divide-by-16) complement
8-11,15-20, 22-25,28,29	3,5,31,32,34, 35,39-42, 44,45,47,48, 50,51	D[0:15]	O	ECL	Parallel data outputs
1,12,27, 39,51	4,10,18,30, 36,43,49	V_{CC}	-	-	Most positive supply
2,5,13,14,21, 26,35	7,46	V_{TT}	-	-	DCFL negative supply
36,42,43, 46,49	33	V_{EE}	-	-	SCFL negative supply
3,6,32-34,37, 38,40,41,50	1,2,9,11-16,22,24-27,37,38,52	NC	-	-	Do not connect, leave open
4,7	28,29	Test	-	-	Test inputs. Used in factory for testing, connect to VTT through a resistor
52	23	V_{EE}*	-	-	Heat sink bias, connect to V_{EE}

[1] *Can be used single-ended.*

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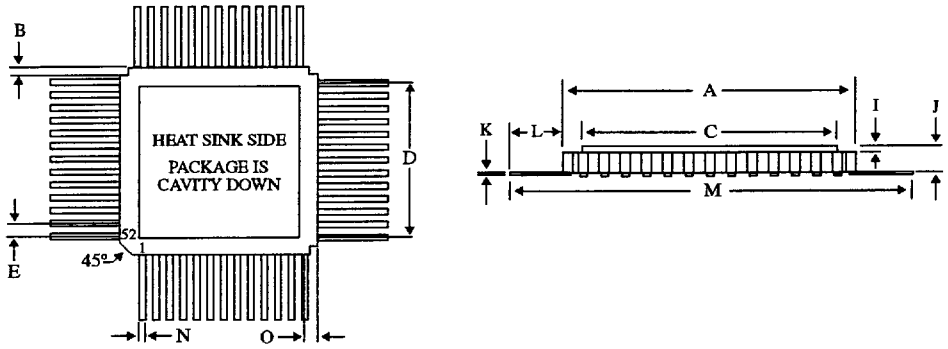
Package Information

52-Pin Ceramic LDCC (F) Package



Item	mm (Min/Max)	in (Min/Max)	Item	mm (Min/Max)	in (Min/Max)
A	18.54/19.56	0.730/0.770	I	0.41/0.61	0.016/0.024
B	1.02/1.52	0.040/0.060	J	2.03/2.79	0.080/0.110
C*	15.49/16.51	0.610/0.650	K*	0.09/0.24	0.003/0.009
D*	15.24 TYP	0.600 TYP	L	4.57/5.34	0.180/0.210
E	1.27 TYP	0.050 TYP	M	27.69/30.22	1.090/1.190
			N	0.36/0.56	0.014/0.022
			O	1.75/1.90	0.069/0.075

** At package body.*
Notes: 1) Drawings not to scale
2) Packages: Ceramic (alumina); Heat Sinks: Copper Tungsten; Leads: Alloy 42 with gold plating.

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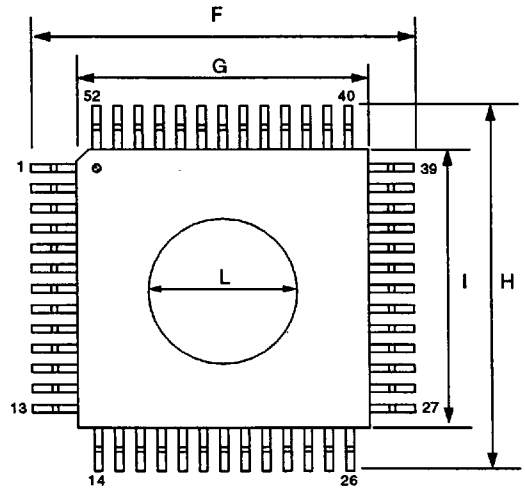
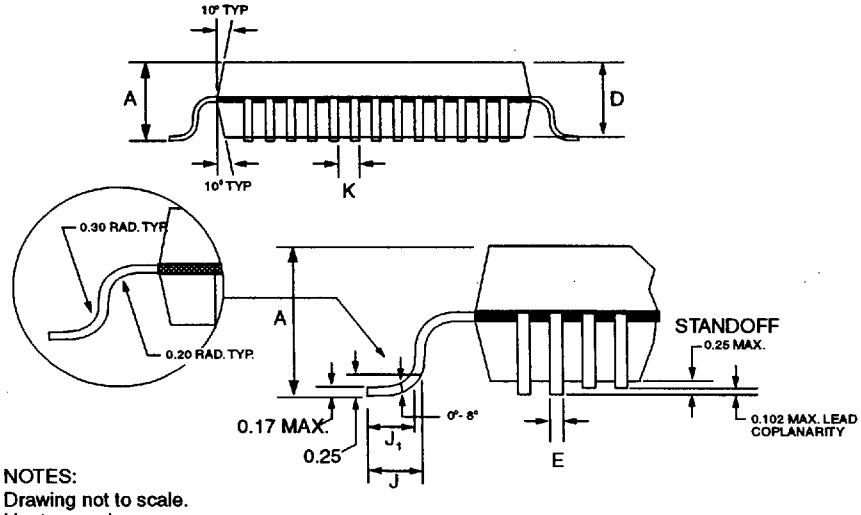
Data Sheet

2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

52 Pin PQFP (QH) Package



Item	*mm*	*Tol.*
A	2.35	MAX
D	2.00	+.10 / -.05
E	0.35	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J	0.88	+.15 / -.10
J1	0.80	+.15 / -.10
K	1.00	BASIC
L	5.84	±.50 DIA.



NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

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Thermal Considerations

The VS8061 and VS8062 are available in ceramic LDCC and thermally enhanced plastic quad flatpacks. These packages have been enhanced to improve thermal dissipation through low thermal resistance paths from the die to the exposed surface of the heat spreader. The thermal resistance of the two packages is shown in the following table

Table 7: Thermal Resistance

Symbol	Description	F Pack	QH Pack	Units
θ_{jc}	Thermal resistance from junction to case.	1.3	2.1	°C/W
θ_{ca}	Thermal resistance from case to ambient still air including conduction through the leads.	18.5	30.0	°C/W

Thermal Resistance with Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

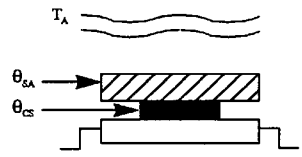
Table 8: Thermal Resistance with Airflow

Airflow	θ_{ca} for F Pack (case to ambient)	θ_{ca} for QH Pack	Units
100 lfpm	15.9	24	°C/W
200 lfpm	14.9	21	°C/W
300 lfpm	14.2	19	°C/W
500 lfpm	13.3	15	°C/W

Thermal Resistance with Heat Sink

The determination of appropriate heat sink to use is as shown below, using the VS8061 in QH package as an example.

Figure 11: VS8061 in QH Package



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The worst case temperature rise from case to ambient is given by the equation:

$$\Delta T = P_{(MAX)}(\theta_{SA} + \theta_{CS})$$

where:

θ_{SA} Theta sink to ambient
θ_{CS} Theta case to sink
$T_{A(MAX)}$ Air temperature, user supplied (typically 55° C)
$T_{C(MAX)}$ Case temperature (85°C for Industrial range)
$\Delta T T_C - T_A$
$P_{(MAX)}$ Power (2.0 W for VS8061)

$$\therefore P = \frac{\Delta T}{\Sigma\theta} = \frac{T_C - T_A}{\theta_{SA} + \theta_{CS}}$$

$$\theta_{SA} = \frac{\Delta T}{P} - \theta_{CS}$$

If T_A = 55° C and θ_{CS} (user supplied) is typically 0.6° C/W,

$$\theta_{SA} = \frac{(85 - 55)°C}{2W} - 0.6°C/W$$

$$\theta_{SA} = 14.4°C/W$$

Therefore, to maintain the proper case and junction temperature, a heat sink with a θ_{SA} of 14.4° C/W or less must be selected at the appropriate air flow.

Note: the heat spreader is tied to V_{EE} in both the VS8061 and VS8062.

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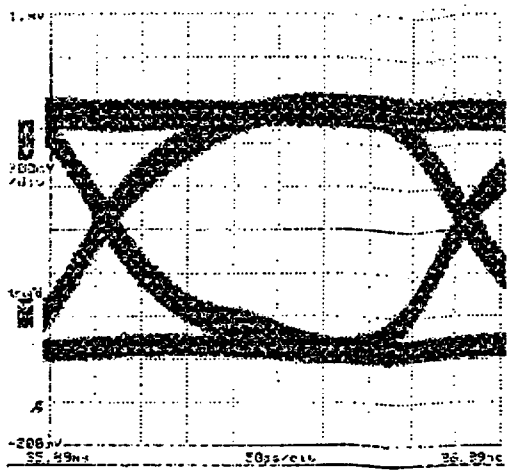
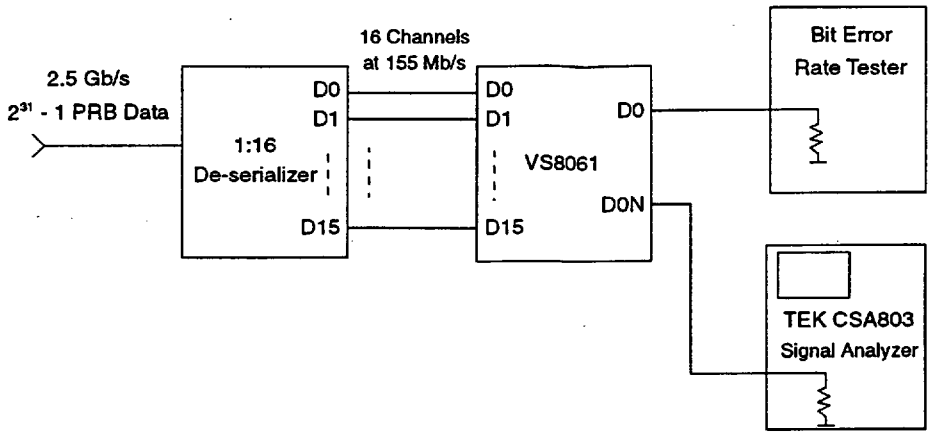
Figure 12: Data Eye From Serial Output of VS8061 in QH Package (D0/D0N)



Amplitude: 200 mV/div
Time Scale: 50 ps/div
Data Rate: 2.5 Gb/s

Figure 13: Measurement Setup



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Data Sheet

2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

Ordering Information

The order number for this product is formed by a combination of the device number, package type, and the operating temperature range.

VS80XX **FC**

Device Type
VS8061 - 2.5 Gb/s 16-bit Multiplexer
VS8062 - 2.5 Gb/s 16-bit Demultiplexer

Package and Temperature
FC: 52 Pin Ceramic Leaded Chip Carrier (LDCC), 0° C ambient to +70° C case
FI: 52 Pin Ceramic Leaded Chip Carrier (LDCC), -40° C ambient to +85° C case
QH: 52.Pin Plastic Quad Flat Pack (PQFP), 0° C ambient to +85° C case

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